IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 4, April 2016

Implementation of Low Power Efficient 32 Point FFT Using Reversible Vedic Multiplier

Syed Hussain Basha[1], Archita K[2], Likhitha Y[3]

Assistant Professor, ECE, Brindavan Institute of Technology & Science, Kurnool, India[1]

Student, ECE, Brindavan Institute of Technology & Science, Kurnool, India[2, 3]

Abstract: In gift state of affairs each technique ought to be fast, effective and. quick Fourier enhance (FFT) is a good algorithmic rule to work out the N purpose DFT. That has nice applications in communication, signal and icon process and instrumentation. Withal the Implementation of FFT needs sizable amount of complicated multiplications, thus to form this method fast and straightforward it is important for a multiplier factor to be quick and wattage economical. To tackle this sort of drawback in religious writing arithmetic could be a competent technique of multiplication. Religious writing arithmetic is that the previous system of arithmetic that successively has associate degree distinctive approach of calculations based mostly in sixteen Sutras. using these sorts of techniques within the calculation algorithms of the coprocessor can cut back the complexity, execution time, area, electricity so forth one amongst the Sanskrit literature of religious writing scientific discipline, changing into a general multiplication resolution, is equally applicable to any or all cases of copie. The traditional multiplication technique needs longer & space on Si than religious writing algorithms. Additional notably process speed will increase with the bit length. This sort of can facilitate finally to hurry up the transmission process task. The individuality through this paper is quick Fourier rework (FFT) style and elegance methodology exploitation religious writing multiplier factor. The aim of this paper is sometimes to supply a strategy to synthesize binary combinative invertible logic circuits for various outputs performs and drop-off a fancy price functions.

Keywords: CI, FFT, GO, Vedic Multiplier, Reversible Logic Gates, Quantum Cost, NG, Optimized Design.

I. INTRODUCTION

With all the advances in technology, several faculty students have tried and can be attending to style multipliers which is able to compromise either of the subsequent style targets -- high speed, low wattage consumption, symmetry of style associate degree therefore less place or perhaps mix of them in an one multiplier factor so creating all of them suited to various high acceleration, low power and tiny VLSI execution.

Direct calculation of distinct Fourier Convert (DFT) needs from the acquisition of N2 complicated propagation businesses wherever N is sometimes the rework size. The FFT algorithmic rule, started a contemporary era in digital indication process by reducing the order of complexness of DFT from N2 to Nlog2N, reduces the quantity of needed complicated épreuve compared to a normal DFT. Since multipliers area unit implausibly wattage hungry factors in VLSI styles concerning they create} about vital power consumption. Therefore, the complicated multiplication functions area unit recognized exploitation Urdhva Tirvagbhyam in Ancient Indian religious writing arithmetic is associate degree economical approach of multiplication. It virtually means that "Vertically and crosswise".

This Sanskrit literature shows a way to handle multiplication of a bigger range (N x N, of N bits each) by breaking it into smaller numbers of size (N/2 = n, say) and these smaller numbers will once more be broken into smaller numbers (n/2 each) until we have a tendency to reach number size of (2 x 2) so, simplifying the full multiplication method. The multiplier factor has the advantage that because the range of bits will increase, gate delay and space will increase terribly slowly as compared to different multipliers.

II. EXISTING LITERATURE

Conventional logic design implementation of 2x2 Urdhva Tiryakbhayam multiplier with irreversible logic. Due to this, the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. So to overcome this problem we are going to a reversible logic gates.

III. VEDIC MATHEMATIC

The word “Vedic” springs from the word “Veda” which implies the store-house of all information. Religious writing strategies ideas are often directly applied to pure mathematics, plain and geometry, conics (both differential and essential), and applied math of diverse varieties. The personal appeal of religious writing arithmetic lies within the indisputable fact that it reduces the cumbersome-looking calculations in typical arithmetic to a really modest one. This can be thus since the religious writing formulae area unit claimed to be supported the natural principles on that the human mind works.

Hindu Bharati Krishna Tirtha (1884- 1960), former Jagadguru Sankaracharya of Puri culled a group of sixteen Sutras (aphorisms) and thirteen Sub - Sutras (corollaries) from the Atharva religious text. He established approaches and techniques for amplifying the principles contained within the aphorisms and their corollaries, and known as it religious writing Mathematic.

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 4, April 2016

Vedic arithmetic is one amongst the foremost ancient methodologies employed by Aryans so as to perform mathematical calculations. This consists of algorithms that may boil down giant arithmetic operations to easy mind calculations. The on top of aforementioned advantage stems from {the fact |the terribly fact|the actual fact} that religious writing arithmetic approach is completely totally different and regarded very near the approach an individual's mind works. The efforts place by Jagadguru Hindu Sri Bharati Krishna Tirtha maharajah to introduce religious writing arithmetic to the commoners. Religious writing Algorithms area unit divided into sixteen classes or Sutras that area unit acknowledged and appreciated.

IV. PROPOSED METHOD

URDHVA TIRYAKBAYAM MULTIPLIER:

The multiplier factor is predicated on associate degree algorithmic rule Urdhva-Tiryakbhayam of ancient Indian religious writing arithmetic. The Sanskrit literature is largely vertically and crosswise. The Indo-Aryan words Urdhva stands for "vertical" and Tiryakbhayam stands for "crosswise". These Sutras are historically used for the multiplication of 2 ranges within the decimal number technique.

During this work, applying the similar ideas to the binary numeration system. During this technique the partial merchandise area unit generated at the same time that itself reduces the delay makes this technique quick. Think about 2, 3 bit numbers A and B wherever A = a1a0 and B = b1b0 as shown in Figure one. Firstly, the smallest amount vital bits area unit increased which supply the smallest amount vital little bit of the merchandise (vertical).

Then, the LSB of the number is increased with consequent higher little bit of the multiplier factor and side by, the merchandise of LSB of multiplier factor then following higher little bit of the number (crosswise).

The total offers second little bit of the merchandise and therefore the carry is side within the output of next stage total that is obtained by process the 3 bits with crosswise and vertical multiplication and addition to grant the total and carry. The total is that the conformist little bit of the merchandise and therefore the carry is once more side to consequent stage multiplication and addition of 2 bits except the LSB. The similar method remains till the multiplication of the 2 MSBs to grant the MSB of the merchandise.

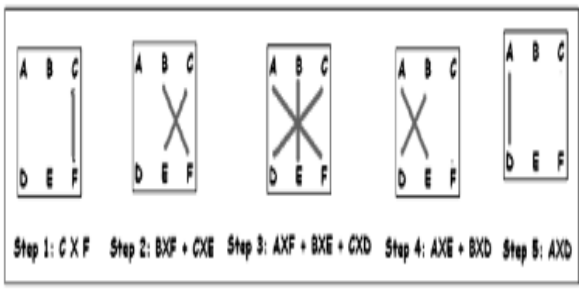

Fig 1: Vertically and Crosswise Multiplication

V. REVERSIBLE MULTIPLIER

Regarding to Moore's law the numbers of transistors will definitely be doubled each eighteen months. so energy old school devices area unit the necessity to possess of the day. The quantity of energy unchaste in a very system carries an instantaneous relationship to the amount of elements erased throughout computation. Alterable circuits area unit those brake lines that don't shed data.

Charles Bennett confirmed that energy loss are often avoided or additionally eliminated if the calculations area unit distributed in reversible logic and likewise verified that circuit created from reversible gates have gotten zero power dissipation. As a result reversible logic looks to be smart in future

The reversible circuit/gate has the subsequent characteristics:

(i) Has equal range of inputs and outputs.
(ii) The gate output that successively isn't used whereas primary output within the circuit, is named trash output.
(iii) The sort that successively is employed as management insight to the gates is certainly known as constant/garbage input
(iv)The fan-out of each gate is reminiscent of one. A repeating routine is used within the event that 2 copies of a proof area unit needed and
(v) The ensuing signal is acyclic. a good style in reversible reason should have the subsequent features:
a) Use minimum quantity of reversible logic entrance
b) Ought to have a lot of less range of garbage results
c) Less range of frequent inputs, and
d) Reduction of quantum expense
e) Low ability style applications.

VI. REVERSIBLE LOGIC GATES

A reversible computer circuit is associate degree n-input, n-output device with matched mapping that helps to retrieve the inputs from the outputs and vice-versa. The most challenges for the reversible logic area unit reducing the facility dissipation, reducing range of gates, delay and quantum price.

But fan-out in reversible circuits is achieved exploitation further gates. A reversible circuit ought to be designed exploitation minimum range of reversible logic gates. From the purpose of read of reversible circuit style, there area unit several parameters for crucial the complexness and performance of circuits.

A. Cnot Gate

The Controlled-NOT gate, or CNOT, takes as input 2 bits (a management bit and a target bit) and performs the operations. If the management bit is about to zero it wills nothing. If it's set to at least one, the target bit is flipped.

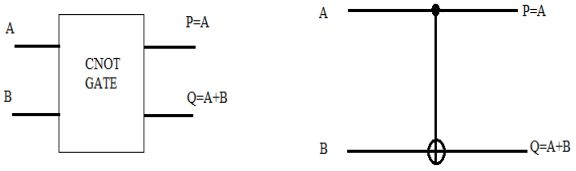

Fig 2: CNOT gate

IJIREEICE
ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526
INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 4, April 2016

B. Peres Gate

Peres gate has input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = A ⊕ B and R=AB ⊕ C. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

Fig 3: Peres gate

C. Hing Gate

It is a 4x4 gate and its logic circuit is as shown within the figure. It's quantum price six. It's used for coming up with ripple carry adders. It will turn out each total and carry in a very single gate so minimizing the rubbish AND circuit counts.

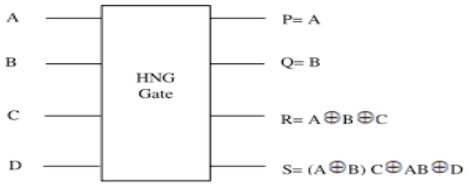

Fig 4: Hing gate

VII. OPTIMIZATION OF THE URDHVA TIRYAKBHAYAM MULTIPLIER

The Reversible 4X4 multiplier factor style emanates coming back from the 2X2 multiplier factor. The diagram of the fourX4 religious writing multiplier factor is sometimes bestowed within the form 4.

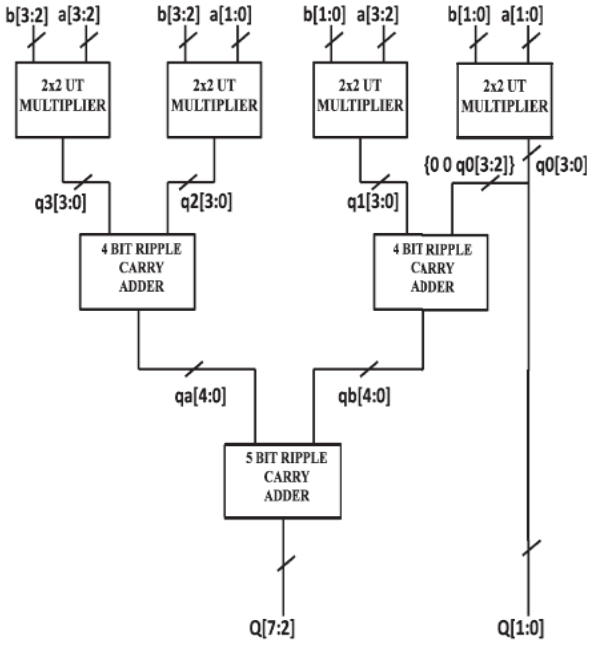

Fig 5: Reversible 2x2 multiplier

It contains many 2X2 Multipliers every of that procures four items as inputs; 2 items from the number and 2 bits from the multiplier factor.

The reduced 2 parts of the output from the primary 2X2 multiplier factor happen to be entrapped because the least costly 2 bits of the ultimate results of copie. 2 zeros area unit concatenated with the higher 2 bits and given whereas input to the ripple carry adder and purchased from the second 2X2 multiplier factor. Likewise the results of the third and therefore the terminal 2X2 multipliers area unit given as advices to the second four bit ripple carry adder. The outputs of those sorts of four bit ripple hold adder's area unit in stomach five bit every that typically have to be compelled to be summed up.

VIII. INTRODUCTION TO FFT

Digital signal process could be a place of science and style that has developed quickly within the last thirty years. This sort of fast development could be results of the many advances in digital computer technology and integrated-circuit design. The digital computers and associated digital hardware of 3 decades agone had been comparatively giant and expensive and, as an impression, their use was restricted to all-purpose non-real-time (off-line) scientific computations and organization applications.

These economical and comparatively quick digital brake lines have created it conceivable to form extremely superior digital systems capable of completing complicated digital signal management functions and tasks, that successively typically area unit too troublesome and too costly to become performed by analog electronic equipment or maybe analog signal process devices. Therefore several of the signal process tasks that were conventionally performed just by analog means that area unit noticed nowadays by more cost effective and sometimes additional trustworthy digital hardware.

The below shown figure is the 16x16 FFT. We can design 32x32 FFT by using 16x16 FFT.

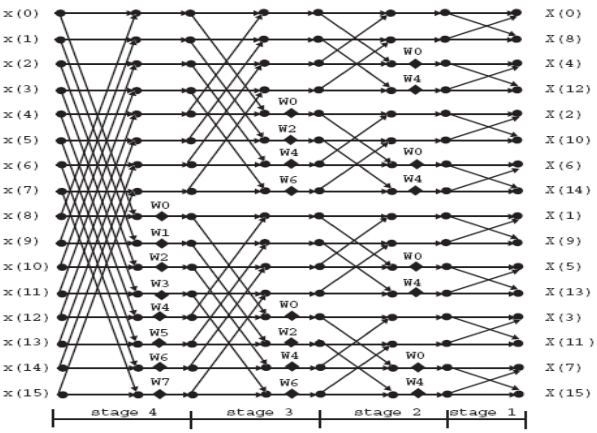

Fig 6: 16 point FFT

IX. EXPERIMENTAL RESULTS

The appearance of the reversible 32x32 multipliers is practically verified using XILINX dokuz. 2i and MODELSIM. The simulation results are while proven in figure.

IJIREEICE

ISSN (Online) 2321 – 2004
ISSN (Print) 2321 – 5526

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH IN ELECTRICAL, ELECTRONICS, INSTRUMENTATION AND CONTROL ENGINEERING
Vol. 4, Issue 4, April 2016

The following are quite design and style constraints for any invertible logic circuits.

1. Invertible logic circuits should include minimum quantum cost.
2. The look can be improved to be able to produce minimum quantity of garbage outputs
3. The reversible logic brake lines must use minimum amount of regular inputs
4. The reversible logic brake lines must use minimum quantity of reversible gates

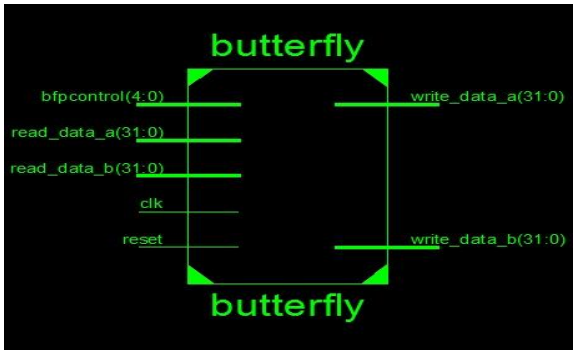

Fig 7: 32x32 REV FFT

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	221	408000	0%
Number of Slice LUTs	3913	204000	1%
Number of fully used LUT-FF pairs	74	4060	1%
Number of bonded IOBs	135	600	22%
Number of BUFG/BUFGCTRL/BUFHCEs	3	200	1%

Fig 8: simulations results for 32x32 FFT

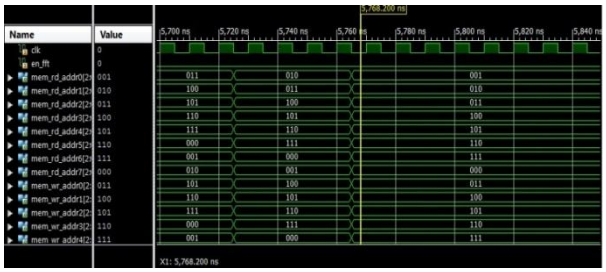

FIG 9: SIMULATION RESULT OF 32X32 FFT

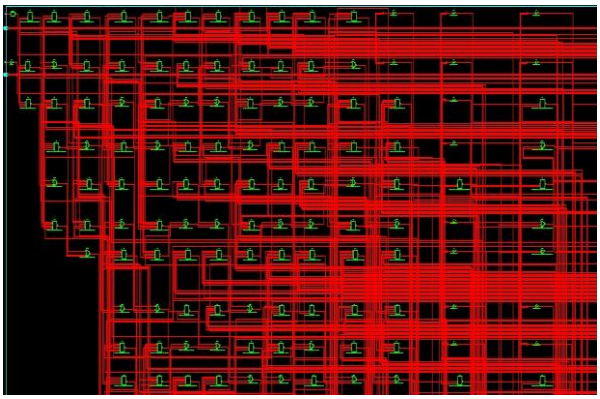

FIG 10: RTL VIEW OF 32X32 REV FFT

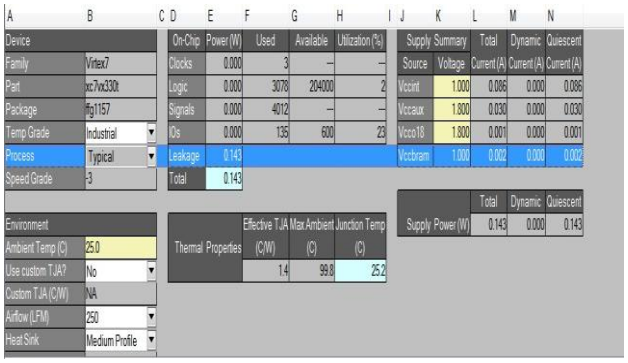

Fig 11: power report of 32x32 REV FFT

Destination	Max (slowest) clk (edge) to PAD	Process Corner	Min (fastest) clk (edge) to PAD	Process Corner	Internal Clock(s)	Clock Phase
write_data_a<0>	8.226 (R)	SLOW	6.897 (R)	FAST	clk_BUFGP	0.000
write_data_a<1>	8.237 (R)	SLOW	6.908 (R)	FAST	clk_BUFGP	0.000
write_data_a<2>	8.275 (R)	SLOW	6.946 (R)	FAST	clk_BUFGP	0.000
write_data_a<3>	8.241 (R)	SLOW	6.912 (R)	FAST	clk_BUFGP	0.000
write_data_a<4>	8.276 (R)	SLOW	6.946 (R)	FAST	clk_BUFGP	0.000
write_data_a<5>	8.396 (R)	SLOW	7.067 (R)	FAST	clk_BUFGP	0.000
write_data_a<6>	8.342 (R)	SLOW	7.013 (R)	FAST	clk_BUFGP	0.000
write_data_a<7>	8.348 (R)	SLOW	7.019 (R)	FAST	clk_BUFGP	0.000
write_data_a<8>	8.534 (R)	SLOW	7.204 (R)	FAST	clk_BUFGP	0.000
write_data_a<9>	8.615 (R)	SLOW	7.285 (R)	FAST	clk_BUFGP	0.000
write_data_a<10>	8.652 (R)	SLOW	7.322 (R)	FAST	clk_BUFGP	0.000
write_data_a<11>	8.448 (R)	SLOW	7.119 (R)	FAST	clk_BUFGP	0.000
write_data_a<12>	8.432 (R)	SLOW	7.102 (R)	FAST	clk_BUFGP	0.000
write_data_a<13>	8.410 (R)	SLOW	7.081 (R)	FAST	clk_BUFGP	0.000
write_data_a<14>	8.585 (R)	SLOW	7.256 (R)	FAST	clk_BUFGP	0.000

Fig 10: timing report of Rev FFT 32 point

X. CONCLUSION

This kind of paper presents the Urdhva Tiryakbhayam Vedic Multiplier recognized using reversible logic gateways. First 2x2 UT multiplier is designed using Peres gate and Feynman door. The ripple carry adders that were required for adding the partial products had been constructed using HNG gateways. This design has large speed, smaller area and less power consumption in comparison with other reversible logic multipliers

REFERENCES

[1] Swami BharatiKrsna Tirtha, Vedic Mathematics. Delhi: Motilal Banarsidass publishers 1965
[2] RakshithSaligram and Rakshith T.R. "Design of Reversible Multipliers for linear filtering Applications in DSP" International Journal of VLSI Design and Communication systems, Dec-12
[3] R. Landauer," Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp.183-191, 1961.
[4] C.H. Bennett, "Logical reversibility of Computation", IBM J. Research and Development, pp.525-532, November 1973.
[5] R. Feynman, "Quantum Mechanical Computers," Optics News, Vol.1l, pp. 11-20, 1985.
[6] H. Thapliyal and M.B. Srinivas, "Novel Reversible Multiplier Architecture Using Reversible TSG Gate", Proc. IEEE International Conference on Computer Systems and Applications, pp. 100-103, March 20 06.
[7] Shams, M., M. Haghparast and K. Navi, Novel reversible multiplier circuit in nanotechnology. World Appl. Sci. J.,3(5): 806-810.
[8] SomayehBabazadeh and MajidHaghparast, "Design of a Nanometric Fault Tolerant Reversible Multiplier Circuit" Journal of Basic and Applied Scientific Research, 2012.
[9] Thapliyal, H., M.B. Srinivas and H.R. Arabnia, 2005, A Reversible Version of 4x4 Bit Array Multiplier with Minimum Gates and Garbage Outputs, Int. Conf. Embedded System, Applications (ESA'05), Las Vegas, USA, pp: 106 114.

[10] H. Thapliyal and M.B. Srinivas, "Reversible Multiplier Architecture Using TSG Gate", Proc. IEEE International Conference on Computer Systems and Applications, pp. 241- 244, March 20 07.
[11] M. Haghparast et al. , "Design of a Novel Reversible Multiplier Circuit using HNG Gate in Nanotechnology," in World Applied Science Journal, Vol. 3, No. 6, pp. 974-978, 2008.
[12] M. S. Islam et al. , "Realization of Reversible Multiplier Circuit," in Information Tech. 1, Vol. 8, No. 2, pp. 117-121, 2005.
[13] K. Navi, M. Haghparast, S. JafaraliJassbi, O. Hashemipour, Design of a novel reversible multiplier circuit using HNG gate, World Sci. 1 3 (6). M. Shams et al., "Novel Reversible Multiplier Circuits in Nanotechnology," in World Applied Science Journal, Vol. 3, No. 5, pp, pp. 806- 810, 2008.
[14] M S Islam, M MRahman, Z Begum and M Z Hafiz, 2009. Low Cost Quantum Realization of Reversible Multiplier Circuit. Information Technology Journal, vol. 8(2), pp. 208-213. Peres, Reversible logic and quantum computers, Phys. Rev. A 32 (1985) 3266-3276.
[15] RakshithSaligram and Rakshith T.R. "Novel Code Converter Employing Reversible Logic", International Journal of Computer Applications (IJCA), August 2012. 781
[16] G Ganesh Kumarand V Charishma, Design of highspeedvedic multiplier using Vedic mathematics techniques, ltn'l J. of Scientific and Research Publications, Vol. 2 Issue 3 March 2012.

BIOGRAPHIES

Mr. Syed Hussain Basha has pursued his B.Tech from Al habeeb College of Engg. & Tech, Hyderabad and M.Tech from Shadaan college of Engg. & Tech, Hyderabad. Presently he is working as Asst. Prof in Dept of ECE in Brindavan Institute of Technology & science, Kurnool. He has published 1 International Journal .His research areas of interest are VLSI system design.

Ms. K. Archita is pursuing her B.Tech in Electronics and Communication Engineering from Brindavan Institute of Technology & science, Kurnool.

Ms. Y. Likhitha is pursuing her B.Tech in Electronics and Communication Engineering from Brindavan Institute of Technology &science, Kurnool.

DOI 10.17148/IJIREEICE.2016.4422